HV-mW™、η-Balance™ PWM Controller Programmable Fsw

FEATURES

- **Programmable Switching Frequency**
- **Proprietary HV-mW™ to Achieve Less than 50mW Standby Power**
- **Proprietary η-Balance™ Control to Boost Light Load Efficiency**
- **Proprietary "Zero OCP/OPP Recovery Gap" Control**
- **Proprietary "Audio Noise Free OCP Compensation"**
- **Built-in Soft Start Function**
- **Pin Floating Protection**
- **Frequency Reduction and Burst Mode Control for Energy Saving**
- **Current Mode Control**
- **Built-in Frequency Shuffling**
- **Built-in Synchronous Slope Compensation**
- **Cycle-by-Cycle Current Limiting**
- **Leading Edge Blanking (LEB)**
- **Constant Power Limiting**
- **VDD OVP & Clamp**
- **VDD Under Voltage Lockout (UVLO)**

APPLICATIONS

Offline AC/DC Flyback Converter for

- **AC/DC Adaptors**
- **Open-frame SMPS**
- **Print Power, Scanners, and Motor Drivers**

GENERAL DESCRIPTION

SF5590 is a high performance, highly integrated current mode PWM controller for medium to large offline flyback power converter applications.

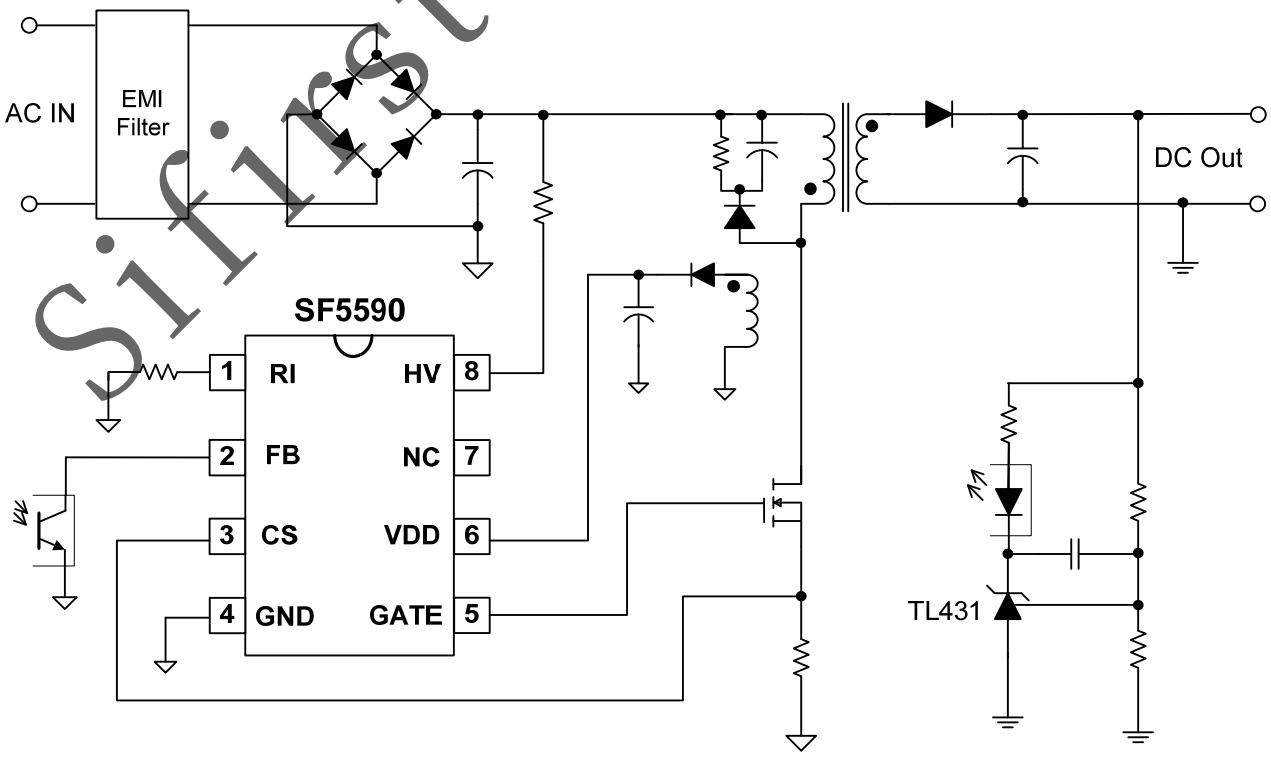
In SF5590, PWM switching frequency with shuffling is externally programmable, which can reduce conduction EMI emission of a power supply. When the output power demands decrease, the IC decreases switching frequency based on the proprietary ***η-Balance™*** control to boost power conversion efficiency at the light load. SF5590 also integrates proprietary ***HV-mW™*** technology to achieve less than 50mW standby power.

SF5590 can achieve "***Zero OCP/OPP Recovery Gap***" using SiFirst's proprietary control algorithm. SF5590 also has built in proprietary "***Audio Noise Free OCP Compensation***", which can achieve constant power limiting and can achieve audio noise operation at heavy loading when line input is 90VAC.

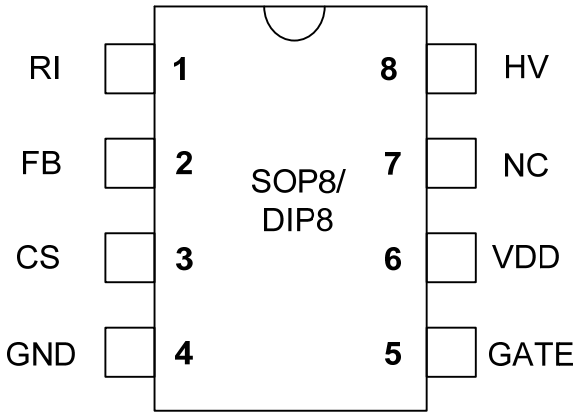
SF5590 integrates functions and protections of Under Voltage Lockout (UVLO), VDD Over Voltage Protection (OVP), Cycle-by-cycle Current Limiting (OCP), Pin Floating Protection, Over Load Protection (OLP), Soft Start, Gate Clamping, VDD Clamping, etc. In SF5590, the protection functions are auto-recovery mode protection.

SF5590 is available in SOP8 and DIP8 packages.

TYPICAL APPLICATION



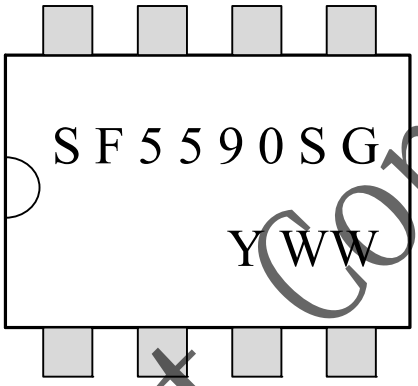
Pin Configuration



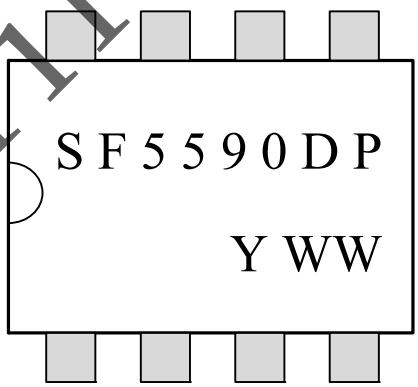
Ordering Information

Part Number	Top Mark	Package		Tape & Reel
SF5590SG	SF5590SG	SOP8	Green	
SF5590SGT	SF5590SGT	SOP8	Green	Yes
SF5590DP	SF5590DP	DIP8	RoHS	

Marking Information

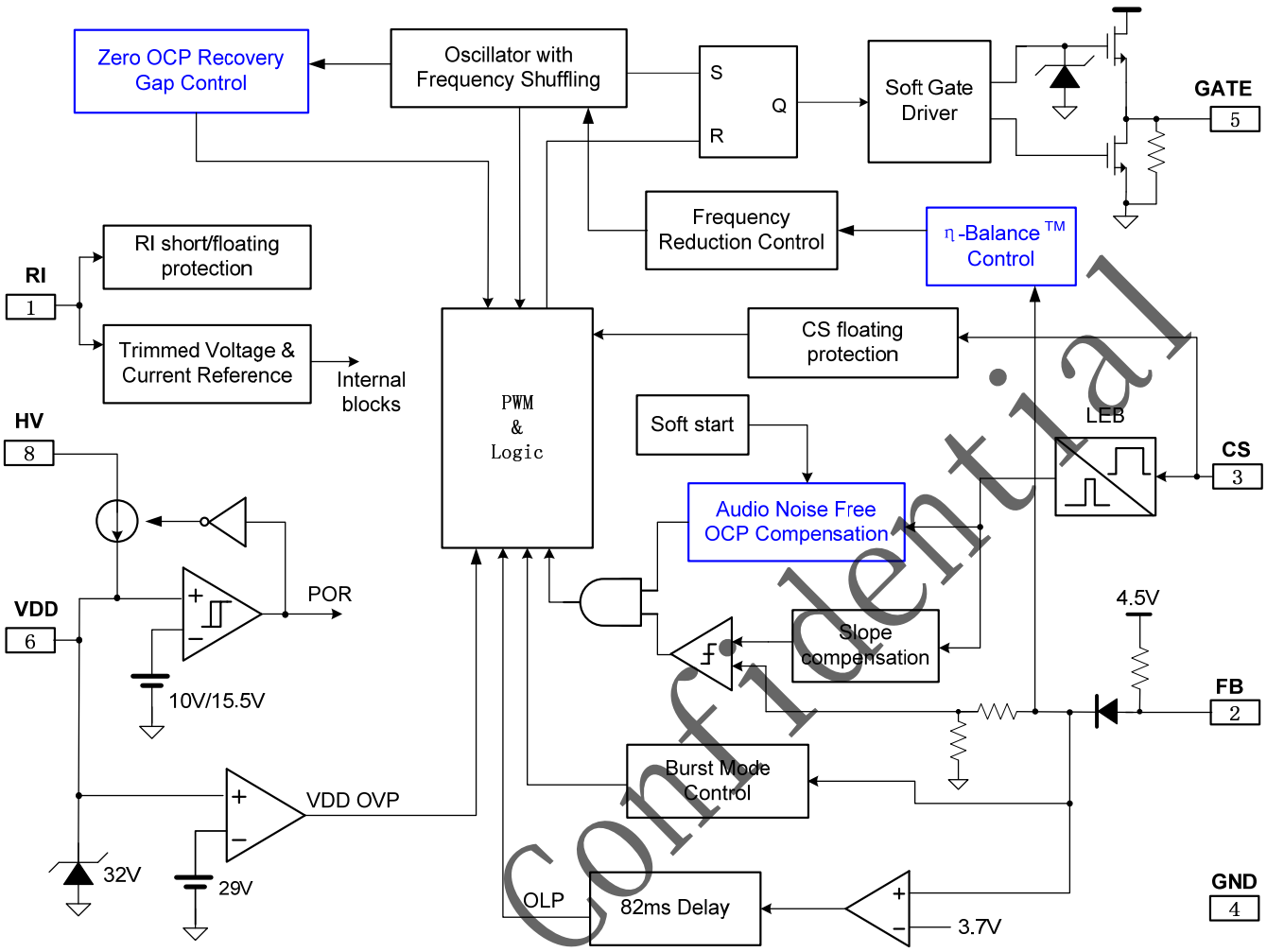


YWW: Year&Week code



YWW: Year&Week code

Block Diagram



Pin Description

Pin Num	Pin Name	I/O	Description
1	RI	I	Set the switching frequency by connecting a resistor between RI and GND. This pin has floating/short-to-GND protection.
2	FB	I	Voltage feedback pin. The loop regulation is achieved by connecting a photo-coupler to this pin. PWM duty cycle is generated by this pin voltage and the current sense signal at Pin 3.
3	CS	I	Current sense input pin.
4	GND	P	IC ground pin.
5	GATE	O	Totem-pole gate driver output to drive the external MOSFET.
6	VDD	P	IC power supply pin.
7	NC	-	No connection.
8	HV	P	This pin connects to bulk capacitor for high voltage startup.

Absolute Maximum Ratings (Note 1)

Parameter	Value	Unit
HV Voltage range	-0.3 to 700	V
VDD DC Supply Voltage	32	V
VDD DC Clamp Current	10	mA
GATE pin	20	V
FB, RI, CS voltage range	-0.3 to 7	V

Package Thermal Resistance (DIP-8)	90	°C/W
Package Thermal Resistance (SOP-8)	150	°C/W
Maximum Junction Temperature	150	°C
Operating Temperature Range	-40 to 85	°C
Storage Temperature Range	-65 to 150	°C
Lead Temperature (Soldering, 10sec.)	260	°C
ESD Capability, HBM (Human Body Model) (Except HV Pin)	3	kV
ESD Capability, MM (Machine Model)	250	V

Recommended Operation Conditions (Note 2)

Parameter	Value	Unit
Supply Voltage, VDD	11 to 26	V
Operating Frequency	50 to 130	kHz
Operating Ambient Temperature	-40 to 85	°C

ELECTRICAL CHARACTERISTICS

(T_A = 25°C, VDD=18V, RI=100K Ohm, if not otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
High Voltage Supply Voltage Section (HV Pin)						
I_HV	HV Current Source	VDD=2V, HV=500V	2	3.5	5	mA
I_HV_leak	HV leakage current	VDD=18V, HV=500V			10	uA
Supply Voltage Section (VDD Pin)						
I_Startup	VDD Start up Current	VDD =12.5V, Measure current into VDD		5	20	uA
I_VDD_Op	Operation Current	V_{FB}=3V,CL=1nF		2	3.5	mA
UVLO(ON)	VDD Under Voltage Lockout Exit (Startup)		14.5	15.5	16.5	V
UVLO(OFF)	VDD Under Voltage Lockout Enter		9	10	11	V
VDD_OVP	VDD Over Voltage Protection trigger		27	29	31	V
V_{DD}_Clamp	VDD Zener Clamp Voltage	I(V_{DD}) = 7mA		32		V
T_Softstart	Soft Start Time			4		mSec
Feedback Input Section(FB Pin)						
V_{FB}_Open	FB Open Voltage			4.5		V
I_{FB}_Short	FB short circuit current	Short FB pin to GND, measure current		0.4		mA
A_{VCS}	PWM Input Gain	$\Delta V_{FB}/\Delta V_{cs}$		1.6		V/V
VFB_min_duty	FB under voltage gate clock is off.			1.1		V
V_{TH}_PL	Power Limiting FB Threshold Voltage			3.7		V
T_D_PL	Power limiting Debounce Time	Note 3		82		mSec
Z_{FB}_IN	Input Impedance			5		Kohm
Current Sense Input Section (CS Pin)						
Vth_OC_min	Internal current limiting threshold	Zero duty cycle	0.70	0.75	0.80	V
Vth_OC_max	Internal current limiting threshold			1		V
T_blanking	SENSE Input Leading Edge Blanking Time			250		nSec
T_D_OC	Over Current Detection and Control Delay	CL=1nF at GATE,		90		nSec
Oscillator Section (RI Pin)						

F_{OSC}	Normal Oscillation Frequency		60	65	70	KHz
RI_range	Operating RI Range		50	100	150	Kohm
V_RI_open	RT open voltage			2.0		V
ΔF(shuffle)/Fosc	Frequency shuffling range	Note 4	-4		4	%
Δf_Temp	Frequency Temperature Stability	-20°C to 100 °C (Note 4)		5		%
Δf_VDD	Frequency Voltage Stability	VDD = 12-25V,		5		%
Duty_max	Maximum Duty cycle		75	80	85	%
F_BM	Burst Mode Base Frequency			22		KHz
Gate Drive Output (GATE Pin)						
VOL	Output Low Level	Io = 20 mA (sink)			0.3	V
VOH	Output High Level	Io = 20 mA (source)	11			V
VG_Clamp	Output Clamp Voltage Level	VDD=24V		16		V
T_r	Output Rising Time	CL = 1nF		120		nSec
T_f	Output Falling Time	CL = 1nF		40		nSec

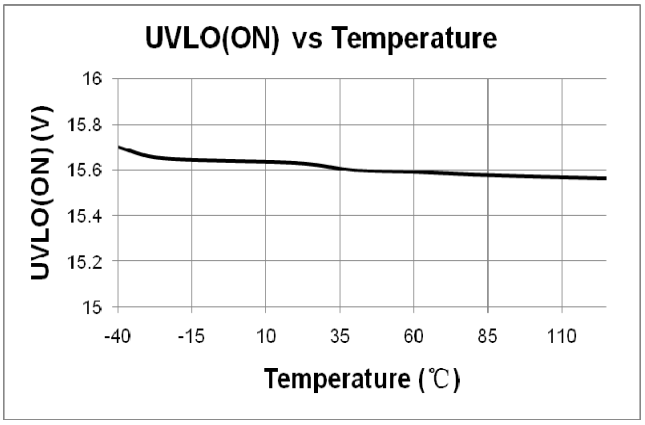
Note 1. Stresses beyond those listed under **"**Absolute Maximum Ratings**"** may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

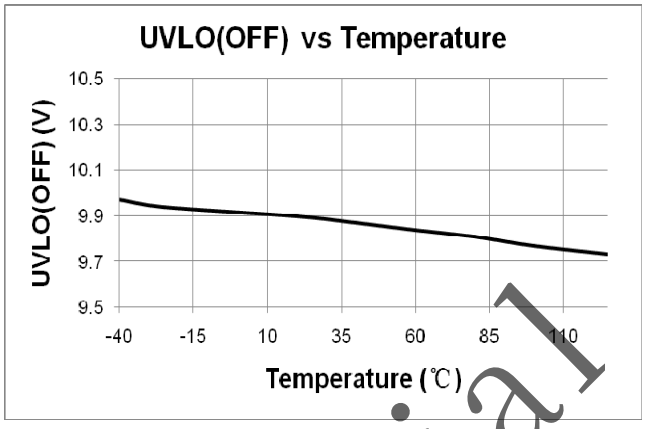
Note 2. The device is not guaranteed to function outside its operating conditions.

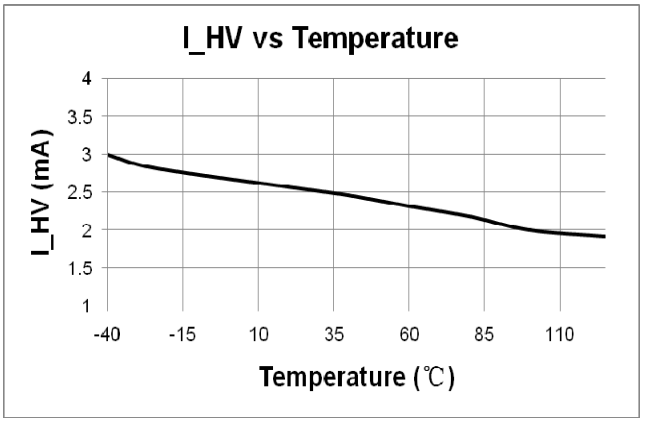
Note 3. The OLP debounce time is proportional to the period of switching cycle.

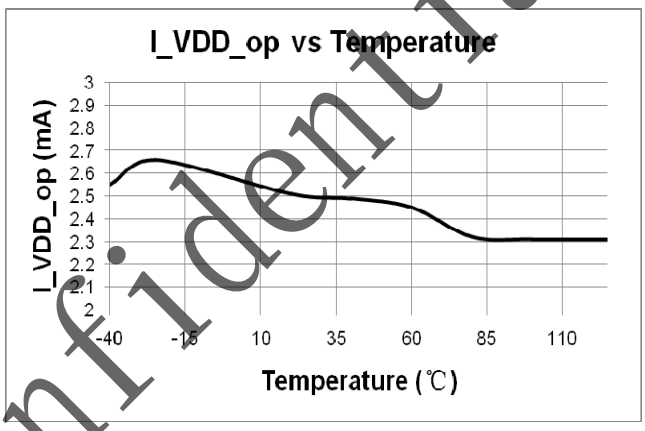
Note 4. Guaranteed by design.

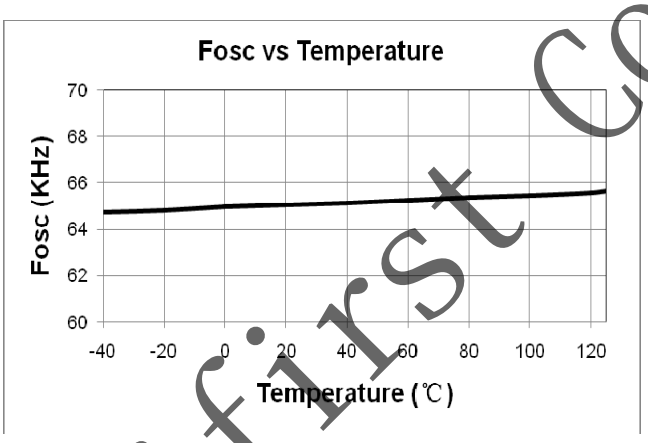
CHARACTERIZATION PLOTS

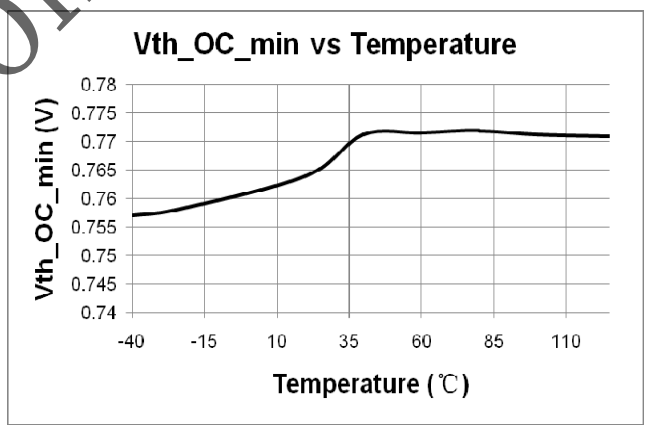


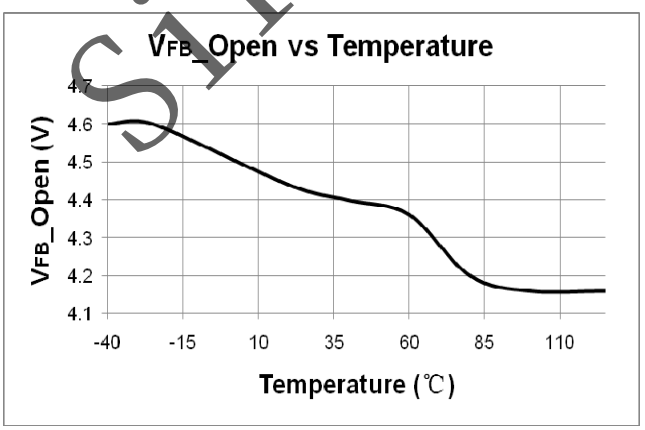


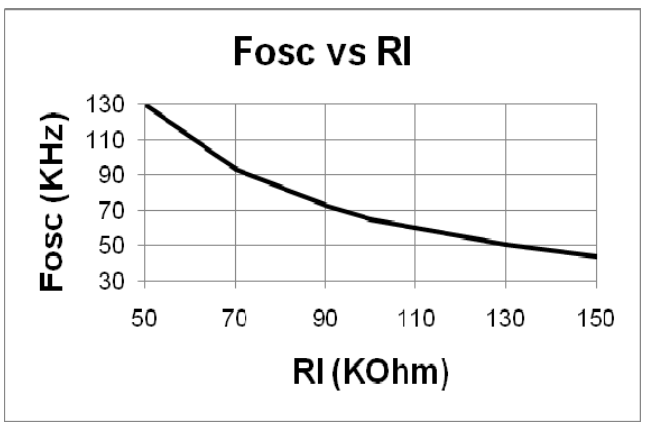












OPERATION DESCRIPTION

SF5590 is a high performance, highly integrated current mode PWM controller for medium to large offline flyback power converter applications.

◆ Proprietary HV-mW™ Technology to Achieve Less than 50mW Standby Power

SF5590 Integrates proprietary *HV-mW™* technology to achieve less than 50mW standby power. The core of *HV-mW™* technology is related a built-in 700V startup circuit and standby control. Fig.1 shows the high voltage (HV) startup circuit for SF5590 applications. The HV pin is connected to the line input or bulk capacitor through a resistor. During startup, the internal startup circuit is enabled and a HV current source charges the VDD hold up capacitor Cdd through Rst. When VDD reaches UVLO turn-on voltage of 15.5V(typical), SF5590 begins switching and the IC current consumed increased to 2mA (typical). The hold-up capacitor Cdd continues to supply VDD before the energy can be delivered from auxiliary winding Na. During this process, VDD must not drop below UVLO turn-off voltage (typical 10V).

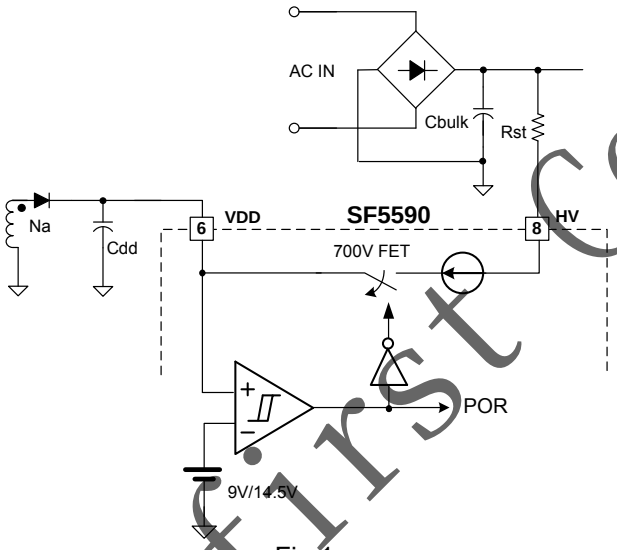


Fig.1

In general application, Rst is recommended to be larger than 30KΩ to limit the startup current.

◆ Low Operating Current

The operating current in SF5590 is as small as 2mA (typical). The small operating current results in higher efficiency and reduces the VDD hold-up capacitance requirement.

◆ Soft Start

SF5590 features an internal 4ms (typical) soft start that slowly increases the threshold of cycle-by-cycle current limiting comparator during startup sequence. It helps to prevent transformer saturation and reduce the stress on the secondary diode during startup. Every restart attempt is followed by a soft start activation.

◆ "Zero OCP/OPP Recovery Gap" Control

The definition of OCP or OPP recovery gap of a power adaptor is illustrated in Fig.2. At T0, assuming an adaptor is at full loading mode. If the loading keeps increasing, then the system will output maximum power P_opp, which will trigger OPP protection at the same time. After the OPP protection is triggered, usually the system will enter into the auto-recovery mode, in burst manner. If the system power demand decreases below P_recovery, then system will enter into normal mode again, as shown in Fig.2. The difference between P_opp and P_recovery is defined as "***OPP Recovery Gap***", which can cause system startup failure especially in 90VAC full load startup.

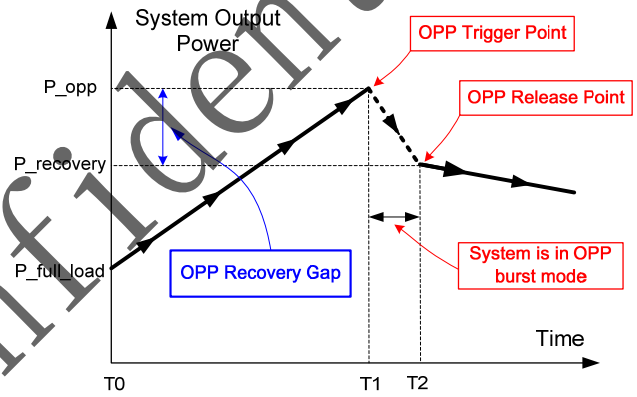


Fig.2

SF5590 can achieve "***Zero OCP/OPP Recovery Gap***" in the whole universal AC input range using SiFirst's proprietary control algorithm.

◆ Synchronous Slope Compensation

InSF5590, the synchronous slope compensation circuit is integrated by adding voltage ramp onto the current sense input voltage for PWM generation. This greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation and thus reduces the output ripple voltage.

◆ Oscillator with Frequency Shuffling

Connecting a resistor from RI pin to GND according to the equation below to program the normal switching frequency:

$$F_{OSC}(KHz) = \frac{6500}{RI(K\Omega)}$$

It can typically operate between 50kHz to 130kHz. To improve system EMI performance, SF5590 operates the system with ±4% frequency shuffling around setting frequency.

◆ Proprietary η-Balance™ Control

The efficiency requirement of power conversion is becoming tighter than before. These new energy

standards focus on the average efficiency of the whole loading range. Therefore, the light load efficiency is becoming more and more important.

In SF5590, a proprietary *η-Balance*^{TM} control is integrated to boost the light load efficiency. As shown in Fig.3, when the loading becomes light, the IC will reduce the PWM switching frequency according to an optimized frequency reduction curve. The specific frequency reduction curve and the power at a frequency are determined by the output of *η-Balance*^{TM} control. For example, P1 is at full load, P2 is at 75% full load, P3 and P4 are 50% and 25% full load respectively. The *η-Balance*^{TM} control can provide higher average efficiency than conventional frequency reduction technique, as illustrated in Fig.3

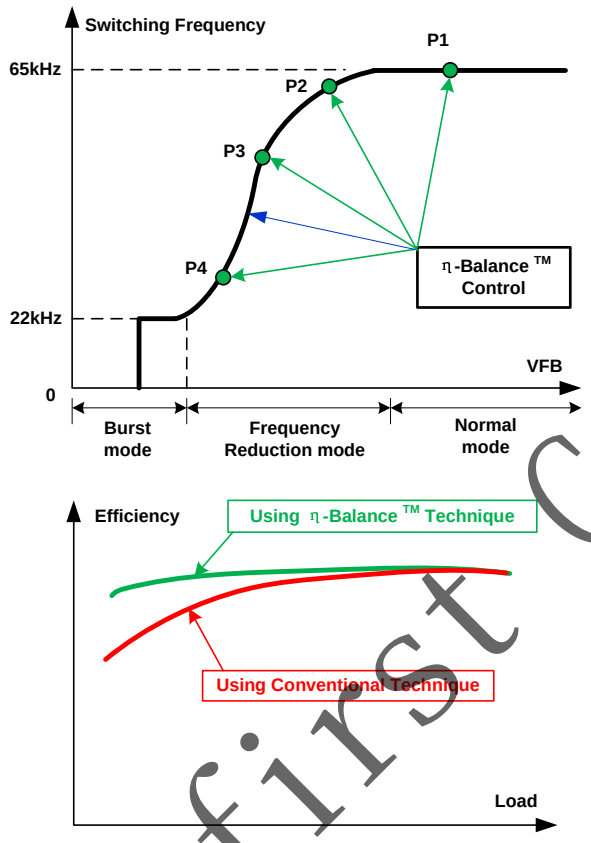


Fig.3

◆ Leading Edge Blanking (LEB)

Each time the power MOSFET is switched on, a turn-on spike occurs across the sensing resistor. The spike is caused by primary side capacitance and secondary side rectifier reverse recovery. To avoid premature termination of the switching pulse, an internal leading edge blanking circuit is built in. During this blanking period (250ns, typical), the PWM comparator is disabled and cannot switch off the gate driver. Thus, external RC filter with a small time constant is enough for current sensing.

◆ Burst Mode Control

When the loading is very small, the system enters into burst mode. When VFB drops below Vskip, SF5590 will stop switching and output voltage starts to drop, which causes the VFB to rise. Once VFB rises above Vskip, switching resumes. Burst mode control alternately enables and disables switching, thereby reducing switching loss in standby mode.

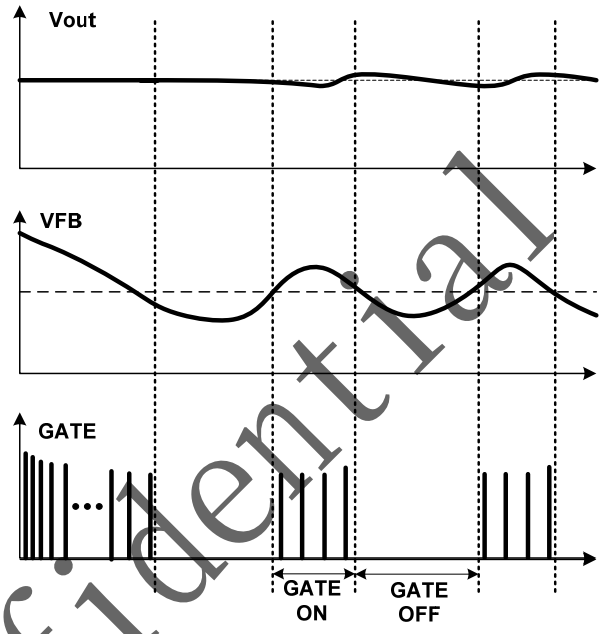


Fig.4

◆ Audio Noise Free OCP Compensation

Conventional OCP compensation may have audio noise issue when AC line is around 90VAC and heavy loading. As shown in Fig.5, when increasing from full load to hiccup load at 90VAC, VFB may oscillate in conventional OCP compensation system. The oscillation can generate large audio noise. In SF5590, a proprietary "Audio Noise Free OCP Compensation" is integrated, which can achieve constant power limiting with no audio noise generated.

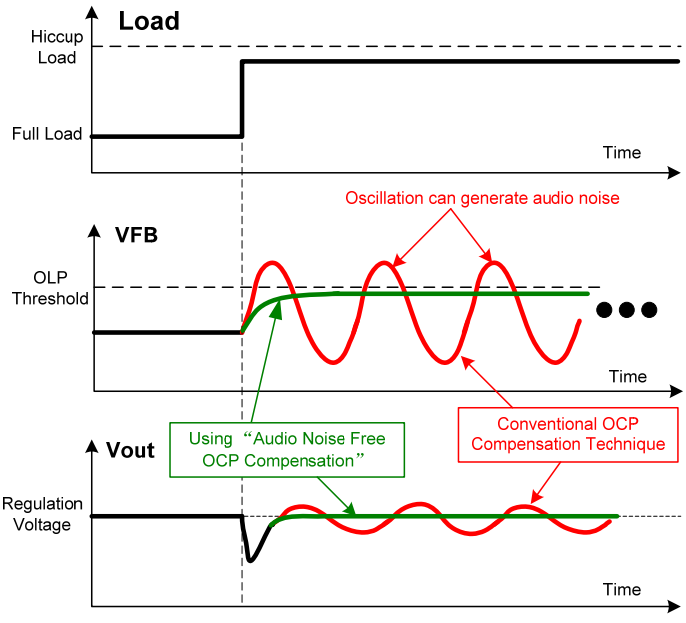


Fig.5

◆ Over Load Protection (OLP) / Over Current Protection (OCP) / Over Power Protection (OPP) / Open Loop Protection (OLP)

When OLP/OCP/OPP/Open Loop occurs, a fault is detected. If this fault is present for more than 82ms (typical), the protection will be triggered, the IC will experience an auto-recovery mode protection, as shown in Fig.6. The 82ms delay time is to prevent the false trigger from the power-on and turn-off transient.

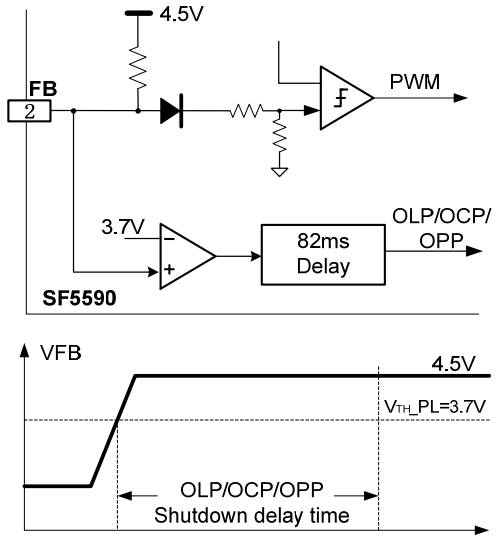


Fig.6

◆ VDD OVP(Over Voltage Protection)

VDD OVP (Over Voltage Protection) is implemented in SF5590 and it is a protection of auto recovery mode protection.

◆ Pin Floating Protection

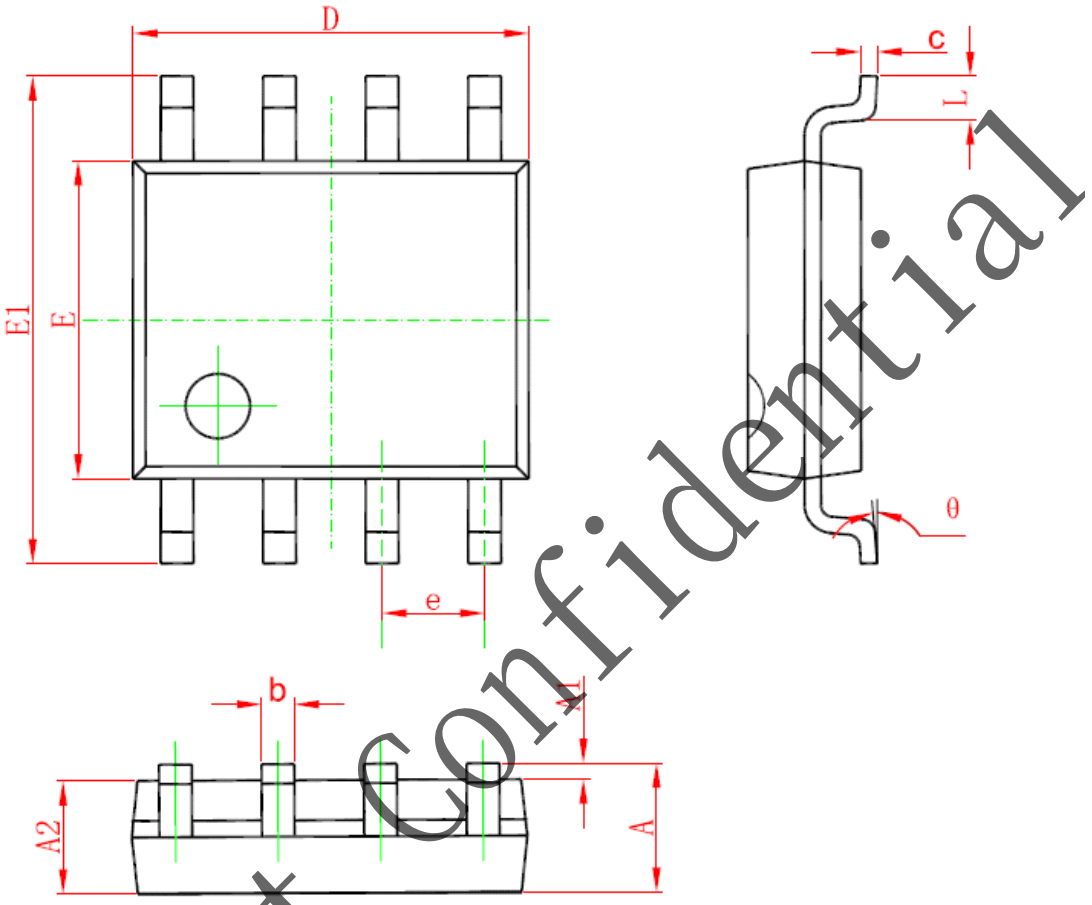
In SF5590, if pin floating situation occurs, the protection is triggered immediately and the system will experience the process of auto-recovery mode protection.

◆ Soft Gate Drive

SF5590 has a fast totem-pole gate driver with 800mA capability. Cross conduction has been avoided to minimize heat dissipation, increase efficiency, and enhance reliability. An internal 16V clamp is added for MOSFET gate protection at higher than expected VDD input. A soft driving waveform is implemented to minimize EMI.

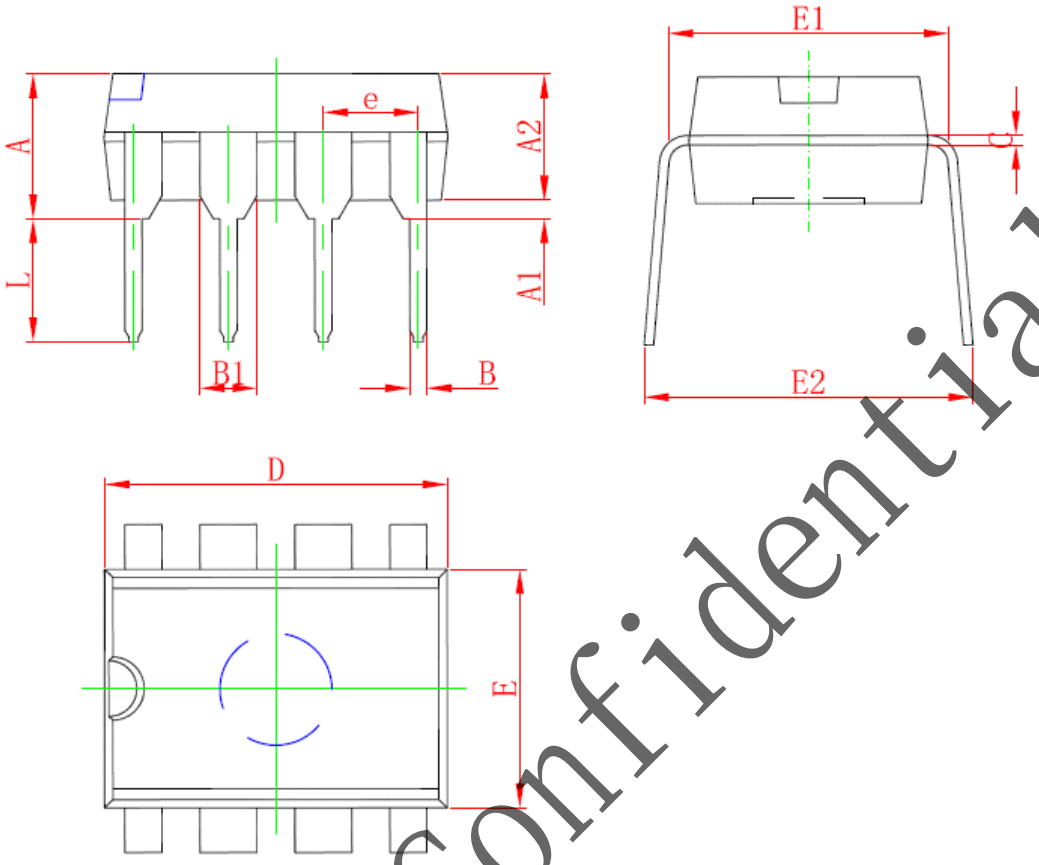
PACKAGE MECHANICAL DATA

SOP8 PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.050	0.250	0.002	0.010
A2	1.250	1.650	0.049	0.065
b	0.310	0.510	0.012	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.150	0.185	0.203
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.05 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

DIP8 PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	3.710	4.310	0.146	0.170
A1	0.510		0.020	
A2	3.200	3.600	0.126	0.142
B	0.380	0.570	0.015	0.022
B1	1.524 (BSC)		0.06 (BSC)	
C	0.204	0.360	0.008	0.014
D	9.000	9.400	0.354	0.370
E	6.200	6.600	0.244	0.260
E1	7.320	7.920	0.288	0.312
e	2.540 (BSC)		0.100 (BSC)	
L	3.000	3.600	0.118	0.142
E2	8.400	9.000	0.331	0.354

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