η-Balance™ Current Mode PWM Controller

FEATURES

- **Proprietary η-Balance™ Control to Boost Light Load Efficiency**
- **Proprietary "Zero OCP/OPP Recovery Gap" Control**
- **Built-in Soft Start Function**
- **Very Low Startup Current**
- **High Voltage CMOS Process with Excellent ESD Protection**
- **Frequency Reduction and Burst Mode Control for Energy Saving**
- **Current Mode Control**
- **Built-in Frequency Shuffling**
- **Programmable Switching Frequency**
- **Built-in Synchronous Slope Compensation**
- **Pins Floating Protection**
- **Cycle-by-Cycle Current Limiting**
- **Built-in Leading Edge Blanking (LEB)**
- **Constant Power Limiting**
- **Audio Noise Free Operation**
- **VDD OVP & Clamp**
- **VDD Under Voltage Lockout (UVLO)**

APPLICATIONS

Offline AC/DC Flyback Converter for

- **AC/DC Adaptors**
- **Open-frame SMPS**
- **Set-Top Box Power Supplies**
- **ATX Standby Power**

GENERAL DESCRIPTION

SF1531S is a high performance, high efficiency, low cost, highly integrated current mode PWM controller for offline flyback converter applications.

PWM switching frequency with shuffling is externally programmable, which can reduce conduction EMI emission of a power supply. When the output power demands decrease, the IC decreases switching frequency based on the proprietary ***η-Balance™*** control to boost power conversion efficiency at the light load. When the current set-point falls below a given value, e.g. the output power demand diminishes, the IC enters into burst mode and provides excellent efficiency without audio noise.

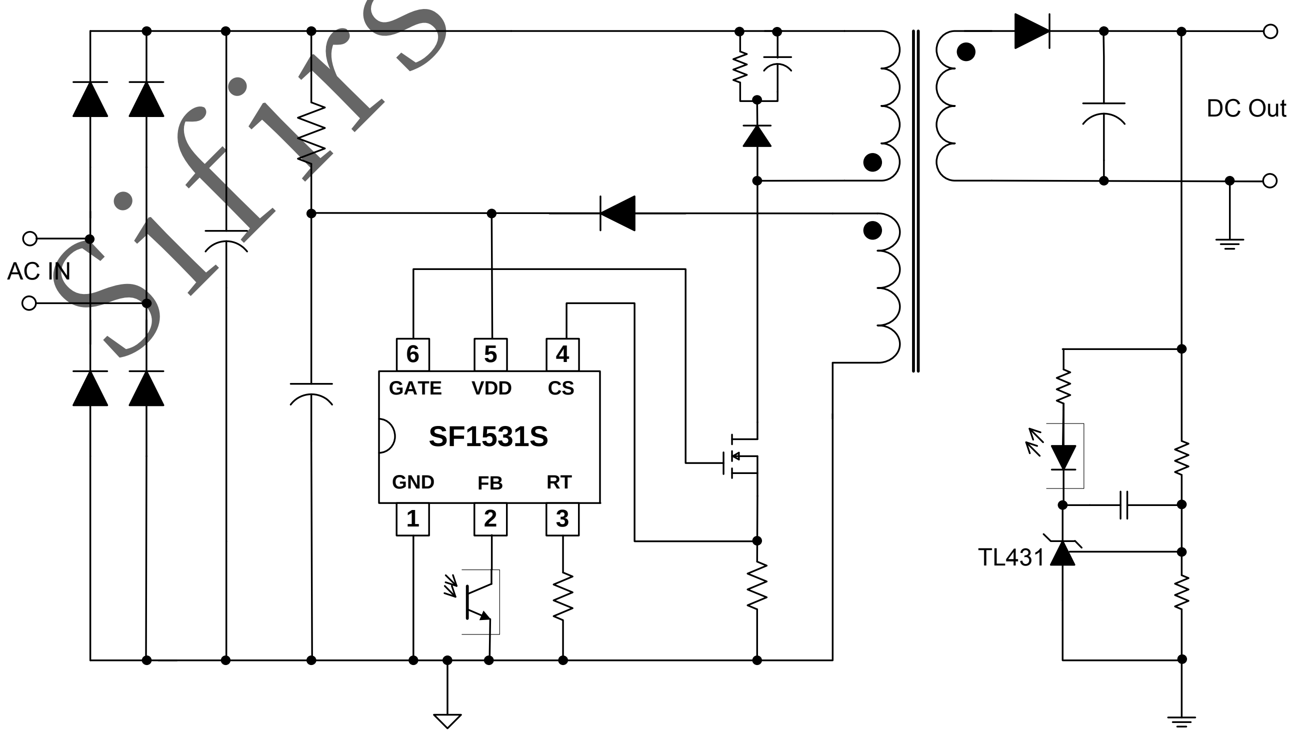
SF1531S can achieve "***Zero OCP/OPP Recovery Gap***" using SiFirst's proprietary control algorithm. Meanwhile, the OCP/OPP variation versus universal line input is compensated.

The IC has built-in synchronized slope compensation to prevent sub-harmonic oscillation at high PWM duty output. The IC also has built-in soft start function to soften the stress on the MOSFET during power on period.

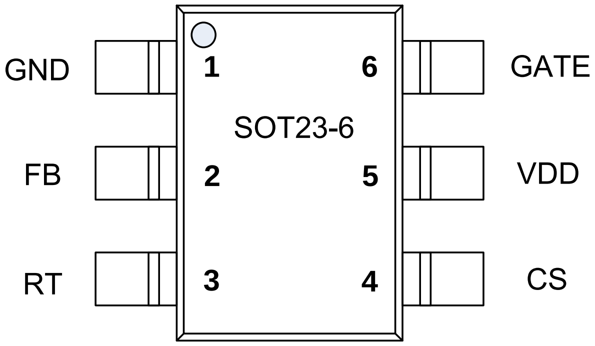
SF1531S integrates functions and protections of Under Voltage Lockout (UVLO), VCC Over Voltage Protection (OVP), Cycle-by-cycle Current Limiting (OCP), All Pins Floating Protection, Over Load Protection (OLP), RT Pin Short-to-GND Protection, Gate Clamping, VCC Clamping, Leading Edge Blanking (LEB).

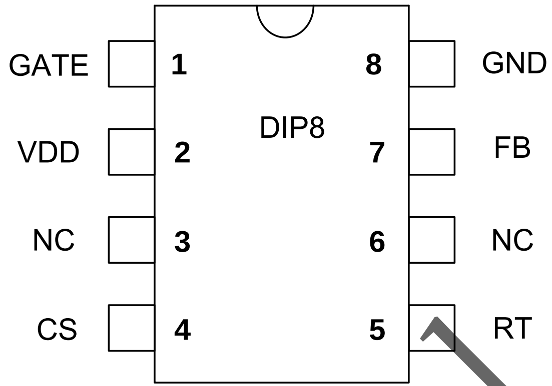
SF1531S is available in SOT23-6, DIP-8 packages.

TYPICAL APPLICATION



Pin Configuration

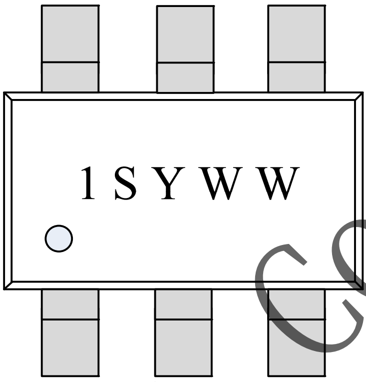




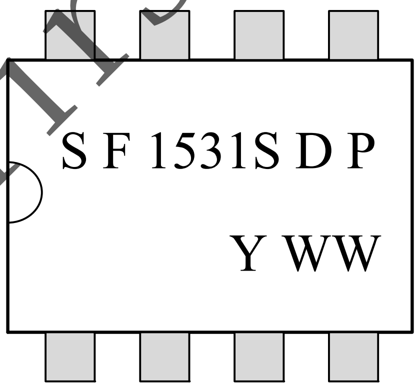
Ordering Information

Part Number	Top Mark	Package		Tape & Reel
SF1531SLGT	.1SYWW	SOT26	Green	Yes
SF1531SDP	SF1531SDP	DIP8	RoHS	

Marking Information

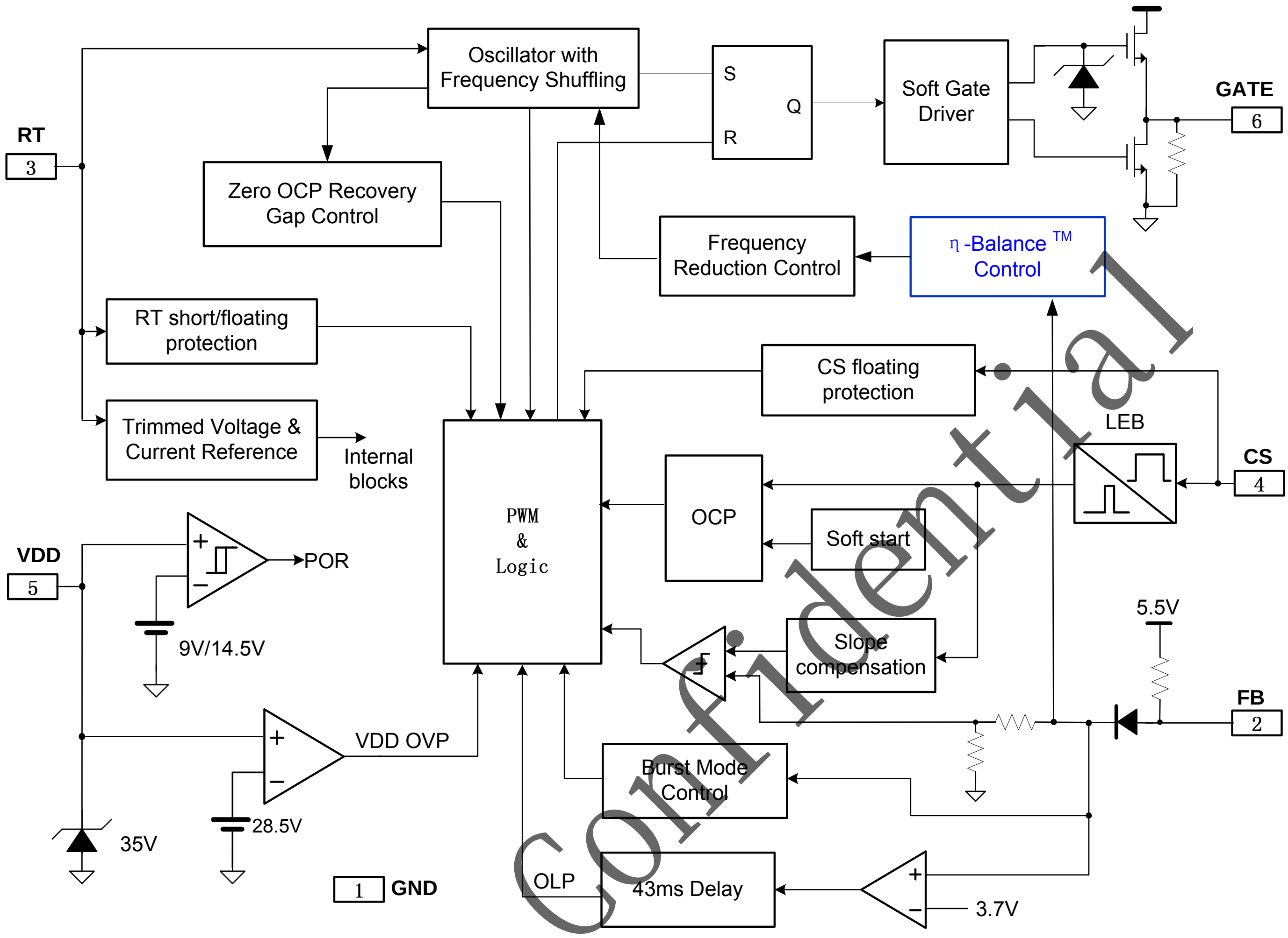


Dot: Pin1 Mark
31:Part number SF1531
YWW: Year&Week Code



YWW: Year&Week code

Block Diagram



Pin Description

Pin Num	Pin Name	I/O	Description
1	GND	P	Ground
2	FB	I	Voltage feedback pin. The loop regulation is achieved by connecting a photo-coupler to this pin. PWM duty cycle is determined by this pin voltage and the current sense signal at Pin 3.
3	RT	I	Set the switching frequency by connecting a resistor between RT and GND. This pin has floating/short-to-GND protection.
4	CS	I	Current sense input pin.
5	VDD	P	IC power supply pin.
6	GATE	O	Totem-pole gate driver output to drive the external MOSFET.

Absolute Maximum Ratings (Note 1)

Parameter	Value	Unit
VDD DC Supply Voltage	35	V
VCC DC Clamp Current	10	mA
GATE pin	20	V
FB, RT, CS voltage range	-0.3 to 7	V
Package Thermal Resistance (SOT-26)	250	°C/W
Package Thermal Resistance (DIP-8)	90	°C/W
Package Thermal Resistance (SOP-8)	150	°C/W

Maximum Junction Temperature	150	^{o}C
Operating Temperature Range	-40 to 85	^{o}C
Storage Temperature Range	-65 to 150	^{o}C
Lead Temperature (Soldering, 10sec.)	260	^{o}C
ESD Capability, HBM (Human Body Model)	3	kV
ESD Capability, MM (Machine Model)	250	V

Recommended Operation Conditions (Note 2)

Parameter	Value	Unit
Supply Voltage, VDD	11 to 25	V
Operating Frequency	50 to 130	kHz
Operating Ambient Temperature	-40 to 85	^{o}C

ELECTRICAL CHARACTERISTICS

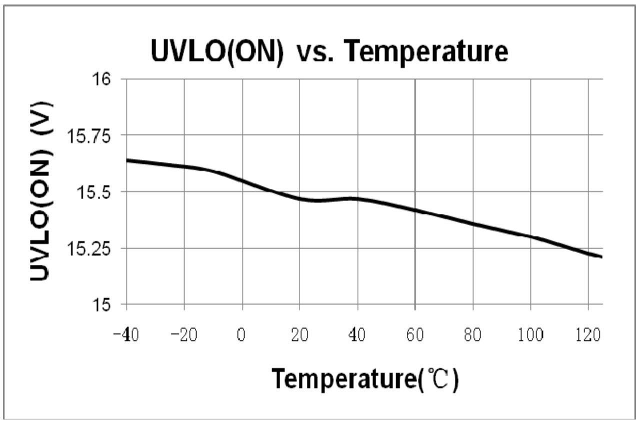
(T_A = 25^{O}C, RT=100K ohm, VDD=18V, if not otherwise noted)

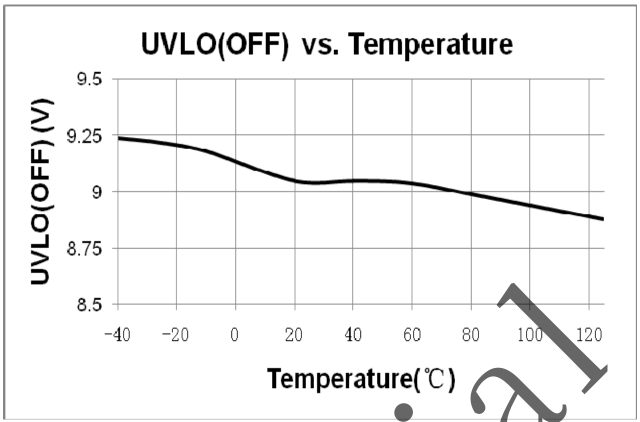
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Supply Voltage Section (VDD Pin)						
UVLO(ON)	VDD Under Voltage Lockout Exit (Startup)		14.5	15.5	16.5	V
UVLO(OFF)	VDD Under Voltage Lockout Enter		8	9	9.8	V
I_Startup	VDD Start up Current	VDD =12.5V, Measure current into VDD		5	20	uA
I_VDD_Op	Operation Current	V_{FB}=3V,CL=1nF		2.5	3.5	mA
VDD_OVP	VDD Over Voltage Protection trigger		26	28	30	V
V_{DD}_Clamp	VDD Zener Clamp Voltage	I(V_{DD}) = 10mA	33.5	35.5	37.5	V
T_Softstart	Soft Start Time			3		mSec
Feedback Input Section(FB Pin)						
V_{FB}_Open	FB Open Voltage			5.5		V
I_{FB}_Short	FB short circuit current	Short FB pin to GND, measure current		1.05		mA
A_{VCS}	PWM Input Gain	$\Delta V_{FB}/\Delta V_{cs}$		2.0		V/V
VFB_min_duty	FB under voltage gate clock is off.			1.0		V
V_{TH}_PL	Power Limiting FB Threshold Voltage			3.6		V
T_D_PL	Power limiting Debounce Time	Note 3		42		mSec
Z_{FB}_IN	Input Impedance			5		Kohm
Current Sense Input Section (CS Pin)						
Vth_OC_min	Internal current limiting threshold	Zero duty cycle	0.70	0.75	0.80	V
T_blanking	SENSE Input Leading Edge Blanking Time			250		nSec
T_D_OC	Over Current Detection and Control Delay	CL=1nF at GATE,		90		nSec
Oscillator Section (RT Pin)						
F_{OSC}	Normal Oscillation Frequency		60	65	70	KHZ
RT_range	Operating RT Range		50	100	150	Kohm
V_RT_open	RT open voltage			2.0		V
ΔF(shuffle)/Fosc	Frequency shuffling range	Note 4	-4		4	%
Δf_Temp	Frequency	-20^{o}C to 100 ^{o}C (Note 4)		5		%

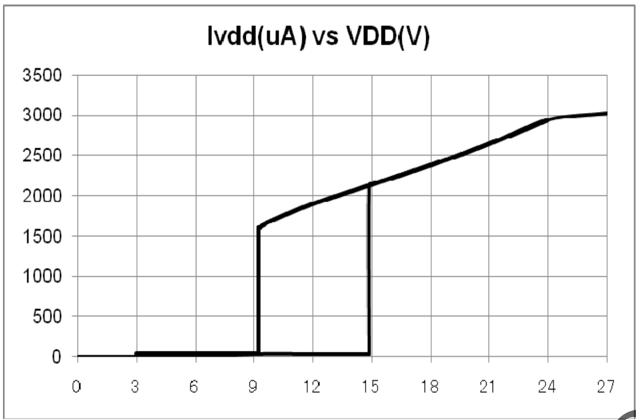
	Temperature Stability					
Δf_VDD	Frequency Voltage Stability	VDD = 12-25V,		5		%
Duty_max	Maximum Duty cycle		75	80	85	%
F_BM	Burst Mode Base Frequency			22		KHZ
Gate Drive Output (GATE Pin)						
VOL	Output Low Level	Io = 20 mA (sink)			1	V
VOH	Output High Level	Io = 20 mA (source)	7.5			V
VG_Clamp	Output Clamp Voltage Level	VDD=24V		16		V
T_r	Output Rising Time	CL = 1nF		220		nSec
T_f	Output Falling Time	CL = 1nF		40		nSec

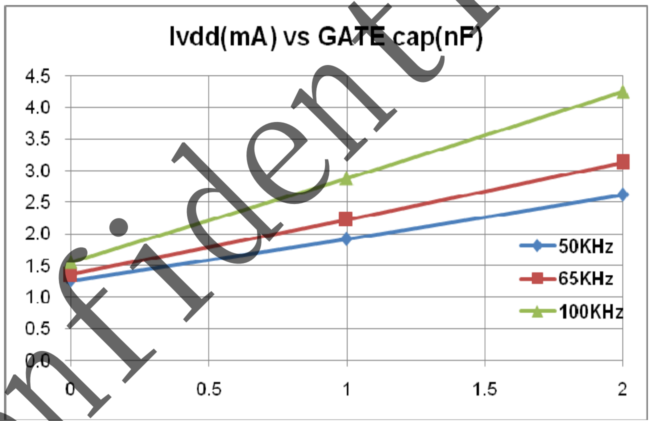
Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
Note 2. The device is not guaranteed to function outside its operating conditions.
Note 3. The OLP debounce time is proportional to the period of switching cycle.
Note 4. Guaranteed by design.

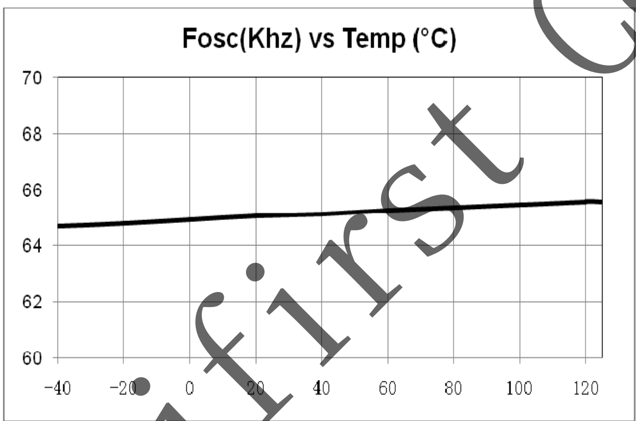
CHARACTERIZATION PLOTS

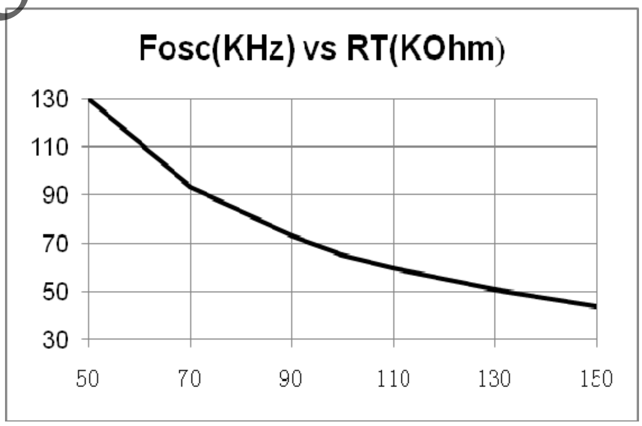


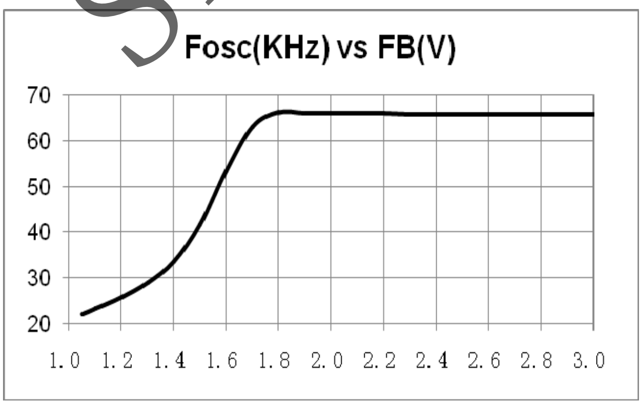


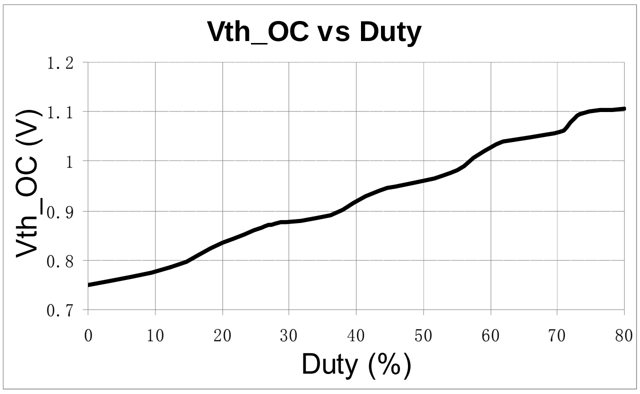












OPERATION DESCRIPTION

SF1531S is a high performance, highly efficiency current mode PWM controller for offline flyback converter applications. The built-in proprietary "Efficiency Equalization" with high level protection features improves the SMPS reliability and performance without increasing the system cost.

◆ UVLO and Startup Operation

Fig.1 shows a typical startup circuitn. Before the IC begins switching operation, it consumes only startup current (typically 5uA) and current supplied through the startup resistor Rst charges the VDD hold-up capacitor Cdd. When VDD reaches UVLO turn-on voltage of 15.5V(typical), SF1531S begins switching and the IC current consumed increased to 2mA (typical). The hold-up capacitor Cdd continues to supply VDD before the energy can be delivered from auxiliary winding Na. During this process, VDD must not drop below UVLO turn-off voltage (typical 9V). The selection of Rst and Cdd should be a trade off between the power loss and startup time.

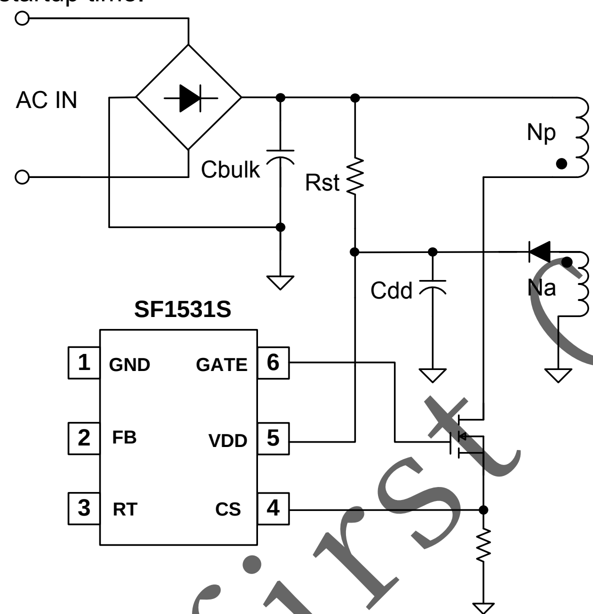


Fig.1

◆ Low Operating Current

The operating current in SF1531S is as small as 1.3mA (typical). The small operating current results in higher efficiency and reduces the VDD hold-up capacitance requirement.

◆ Soft Start

SF1531S features an internal 3ms (typical) soft start that slowly increases the threshold of cycle-by-cycle current limiting comparator during startup sequence. It helps to prevent transformer saturation and reduce the stress on the secondary diode during startup. Every restart attempt is followed by a soft start activation.

◆ "Zero OCP/OPP Recovery Gap" Control

The definition of OCP or OPP recovery gap of a power adaptor is illustrated in Fig.2. At T0, assuming an adaptor is at full loading mode. If the loading keeps increasing, then the system will output maximum power P_opp, which will trigger OPP protection at the same time. After the OPP protection is triggered, usually the system will enter into the auto-recovery mode, in burst manner. If the system power demand decreases below P_recovery, then system will enter into normal mode again, as shown in Fig.2. The difference between P_opp and P_recovery is defined as "***OPP Recovery Gap***", which can cause system startup failure especially in 90VAC full load startup.

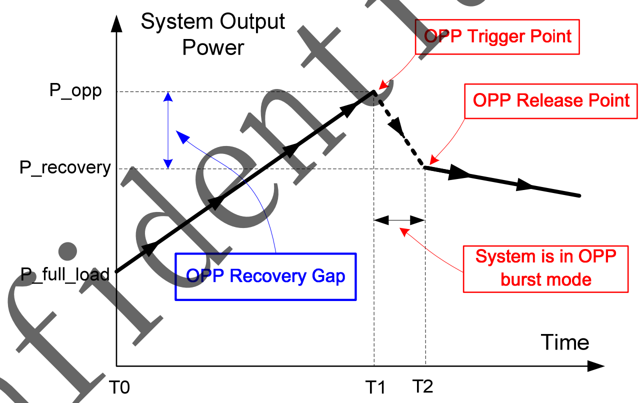


Fig.2

SF1531S can achieve "***Zero OCP/OPP Recovery Gap***" in the whole universal AC input range using SiFirst's proprietary control algorithm.

◆ Synchronous Slope Compensation

InSF1531S, the synchronous slope compensation circuit is integrated by adding voltage ramp onto the current sense input voltage for PWM generation. This greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation and thus reduces the output ripple voltage.

◆ Oscillator with Frequency Shuffling

Connecting a resistor from RT pin to GND according to the equation below to program the normal switching frequency:

$$F_{OSC}(KHz) = \frac{6500}{RT(K\Omega)}$$

It can typically operate between 50kHz to 130kHz. To improve system EMI performance, SF1531S operates the system with ±4% frequency shuffling around setting frequency.

◆ Leading Edge Blanking (LEB)

Each time the power MOSFET is switched on, a turn-on spike occurs across the sensing resistor. The spike is caused by primary side capacitance and secondary side rectifier reverse recovery. To avoid premature termination of the switching pulse, an internal leading edge blanking circuit is built in. During this blanking period (250ns, typical), the PWM comparator is disabled and cannot switch off the gate driver. Thus, external RC filter with a small time constant is enough for current sensing.

◆ Proprietary η-Balance™ Control

The efficiency requirement of power conversion is becoming tighter than before. These new energy standards focus on the average efficiency of the whole loading range. Therefore, the light load efficiency is becoming more and more important.

In SF1531S, a proprietary *η-Balance™* control is integrated to boost the light load efficiency. As shown in Fig.3, when the loading becomes light, the IC will reduce the PWM switching frequency according to an optimized frequency reduction curve. The specific frequency reduction curve and the power at a frequency are determined by the output of *η-Balance™* control. For example, P1 is at full load, P2 is at 75% full load, P3 and P4 are 50% and 25% full load respectively. The *η-Balance™* control can provide higher average efficiency than conventional frequency reduction technique, as illustrated in Fig.3

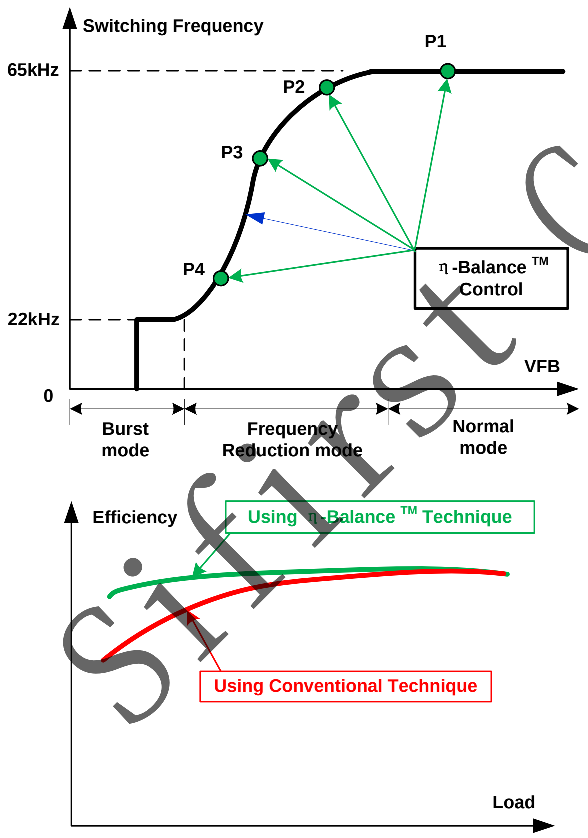


Fig.3

◆ Burst Mode Control

When the loading is very small, the system enters into burst mode. When VFB drops below Vskip, SF1531S will stop switching and output voltage starts to drop, which causes the VFB to rise. Once VFB rises above Vskip, switching resumes. Burst mode control alternately enables and disables switching, thereby reducing switching loss in standby mode.

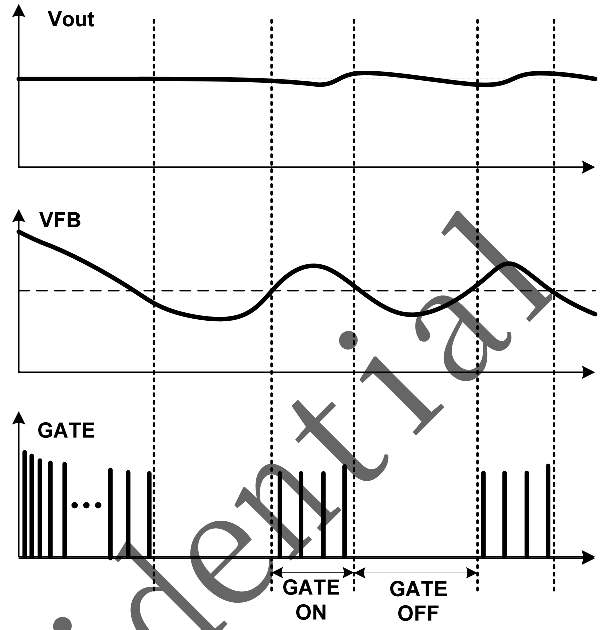


Fig.4

◆ Auto Recovery Mode Protection

As shown in Fig.5, once a fault condition is detected, switching will stop. This will cause VDD to fall because no power is delivered form the auxiliary winding. When VDD falls to UVLO(off) (typical 9V), the protection is reset and the operating current reduces to the startup current, which causes VDD to rise, as shown in Fig.4. However, if the fault still exists, the system will experience the above mentioned process. If the fault has gone, the system resumes normal operation. In this manner, the auto restart can alternatively enable and disable the switching until the fault condition is disappeared.

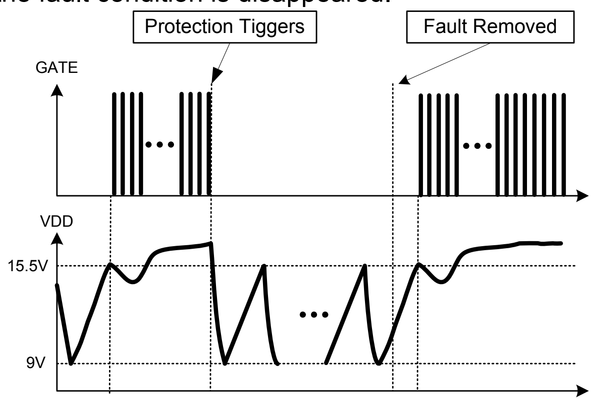


Fig.5

◆ VDD OVP(Over Voltage Protection)

VDD OVP (Over Voltage Protection) is implemented in SF1531S and it is a protection of auto-recovery mode.

◆ Over Load Protection (OLP)

When over load occurs, a fault is detected. If this fault is present for more than 43ms (typical), the protection will be triggered, the IC will experience an auto-recovery mode protection as mentioned above. The 43mS delay time is to prevent the false trigger from the power-on and turn-off transient

◆ All Pins Floating Protection and RT Pin Short-to-GND Protection

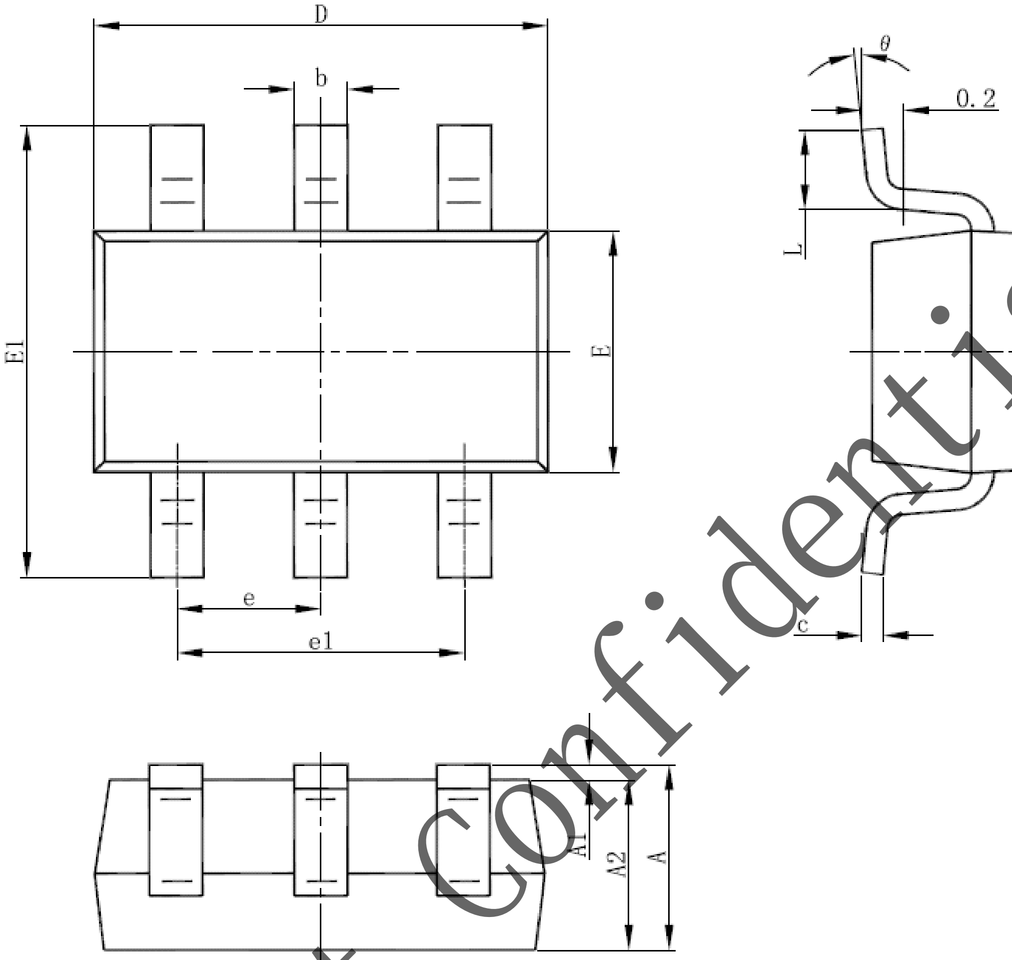
In SF1531S, if pin floating situation or RT pin short-to-GND occurs, the protection is triggered immediately and the system will experience the process of auto-recovery mode protection.

◆ Soft Gate Drive

SF1531S has a fast totem-pole gate driver with 300mA capability. Cross conduction has been avoided to minimize heat dissipation, increase efficiency, and enhance reliability. An internal 16V clamp is added for MOSFET gate protection at higher than expected VDD input. A soft driving waveform is implemented to minimize EMI.

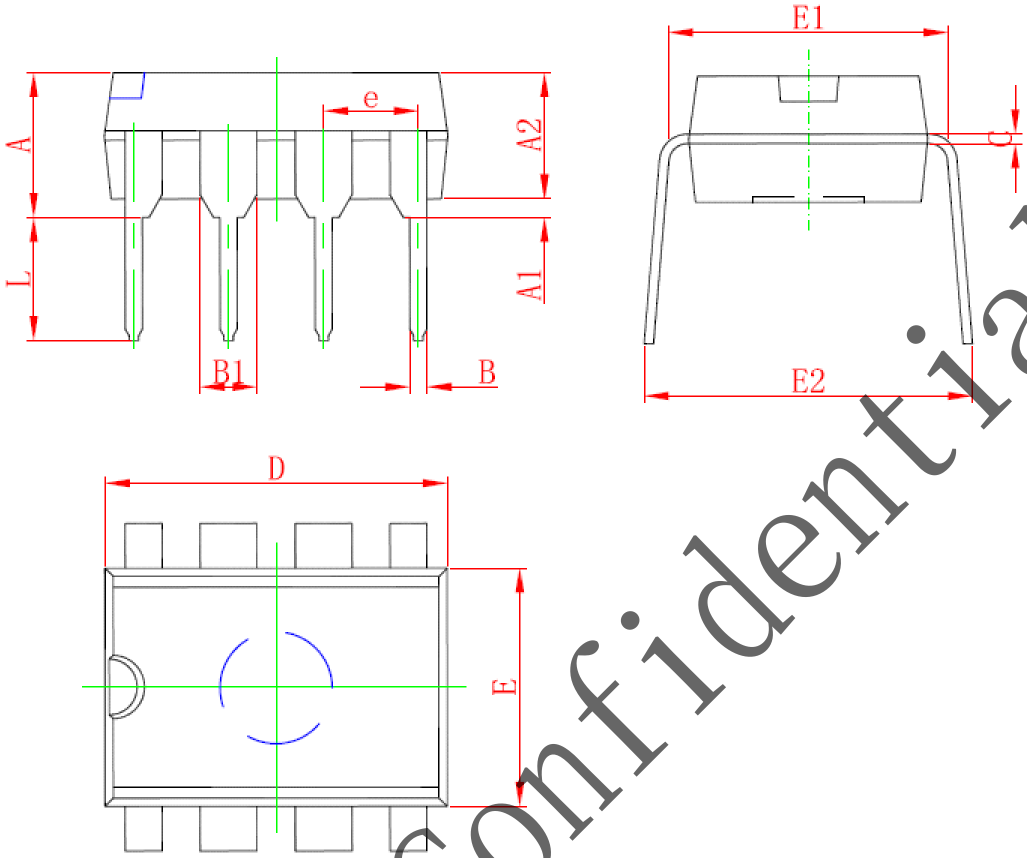
PACKAGE MECHANICAL DATA

SOT-23-6L PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.000	1.300	0.039	0.051
A1	0.000	0.150	0.000	0.006
A2	1.000	1.200	0.039	0.047
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.800	3.020	0.110	0.119
E	1.500	1.700	0.059	0.067
E1	2.600	3.000	0.102	0.118
e	0.950 (BSC)		0.037 (BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0º	8º	0º	8º

DIP8 PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	3.710	4.310	0.146	0.170
A1	0.510		0.020	
A2	3.200	3.600	0.126	0.142
B	0.380	0.570	0.015	0.022
B1	1.524 (BSC)		0.06 (BSC)	
C	0.204	0.360	0.008	0.014
D	9.000	9.400	0.354	0.370
E	6.200	6.600	0.244	0.260
E1	7.320	7.920	0.288	0.312
e	2.540 (BSC)		0.100 (BSC)	
L	3.000	3.600	0.118	0.142
E2	8.400	9.000	0.331	0.354

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